1. A carrier for a semiconductor device, comprising:

a substrate;

at least one conductive trace located on said substrate, said trace including a seat having a cut out portion sized and configured to receive a conductive connecting structure; and

an elastomeric covering material, said material including a gap at a location corresponding to said seat to allow electrical connection of said trace at said seat with a semiconductor die.

2. The carrier of claim 1, wherein said gap separates a first portion of said material from a second portion of said material.

3. The carrier of claim 2, wherein said first and second portions are generally the same size.

4. The carrier of claim 1, further comprising a plurality of said traces.

5. The carrier of claim 4, wherein said traces have a pitch size of about 25 microns to about 500 microns.

6. The carrier of claim 5, wherein said traces have a pitch size of about 150 microns.

7. The carrier of claim 4, wherein each said trace includes a seat having a cut out portion sized and configured to receive a conductive connecting structure.

8. The carrier of claim 7, wherein said seats comprise a metallic surface.

9. The carrier of claim 8, wherein said metallic surface comprises nickel and gold.

10. The carrier of claim 7, wherein said cut out portions extend through said traces to said substrate.

11. The carrier of claim 7, wherein said cut out portions extend through said traces into said substrate.

12. The carrier of claim 7, wherein said cut out portions partially extend through said traces.

13. The carrier of claim 7, wherein each said conductive connecting structure is a solder ball.

14. The carrier of claim 1, wherein said substrate comprises a film.

15. The carrier of claim 14, wherein said film is a polyimide film.

16. The carrier of claim 1, wherein said cut out portions are in the range of 0.005 mm^2 to 1.0 mm^2 in area.

17. A carrier for a semiconductor device, comprising:

a substrate;

a plurality of conductive traces located on said substrate, said traces each including a seat having a cut out portion sized and configured to receive a conductive connecting structure;

an elastomeric covering material, said material including a gap at a location separating a first portion of said material from a second portion of said material and corresponding to said seat to allow electrical connection of said traces with a semiconductor die.

18. The carrier of claim 17, wherein said seats comprise a metallic surface.

19. The carrier of claim 18, wherein said metallic surface comprises nickel and gold.

20. The carrier of claim 17, wherein said first and second portions are generally the same size.

21. The carrier of claim 17, wherein said seats extend through said traces to said substrate.

22. The carrier of claim 17, wherein said seats extend through said traces into said substrate.

23. The carrier of claim 17, wherein said seats partially extend through said traces.

24. The carrier of claim 17, wherein each said conductive connecting structure is a solder ball.

25. The carrier of claim 17, wherein said substrate comprises a film.

26. The carrier of claim 25, wherein said film is a polyimide film.

27. The carrier of claim 17, wherein said cut out portions are in the range of 0.005 mm^2 to 1.0 mm^2 in area.

28. A semiconductor device comprising a semiconductor die electrically connected to a carrier, said carrier comprising:

a substrate;

at least one conductive trace located on said substrate, said trace including a seat having a cut out portion sized and configured to receive a conductive connecting structure; and

an elastomeric covering material, said material including a gap corresponding to said seat to allow electrical connection of said trace with said semiconductor die.

29. The semiconductor device of claim 28, further comprising a plurality of said traces.

30. The semiconductor device of claim 28, wherein each said trace includes a seat sized and configured to receive a conductive connecting structure.

31. The semiconductor device of claim 30, wherein said seats comprise a metallic surface.

32. The semiconductor device of claim 31, wherein said metallic surface comprises nickel and gold.

33. The semiconductor device of claim 30, wherein said seats extend through said traces to said substrate.

34. The semiconductor device of claim 30, wherein said seats extend through said traces into said substrate.

35. The semiconductor device of claim 30, wherein said seats partially extend through said traces.

36. The semiconductor device of claim 28, wherein said substrate comprises a film.

37. The semiconductor device of claim 36, wherein said film is a polyimide film.

38. The semiconductor device of claim 28, wherein said cut out portions are in the range of 0.005 mm^2 to 1.0 mm^2 in area.

39. The semiconductor device of claim 28, wherein said semiconductor die contains a memory circuit.

40. An electronic system, comprising:

a semiconductor die;

a die carrier comprising:

a substrate;

a plurality of conductive traces located on said substrate, each said trace including a seat having a cut out portion receiving a conductive connecting structure; and

an elastomeric covering material, said material including a gap corresponding to said seats, said traces being electrically connected with said semiconductor die through a respective conductive connecting structure provided within said gap; and

a structure for mounting said carrier.

41. The system of claim 40, wherein said structure for mounting said carrier comprises a printed circuit board.

42. The system of claim 40, wherein said seats comprise a metallic surface.

43. The system of claim 42, wherein said metallic surface comprises nickel and gold.

44. The system of claim 40, wherein said seats extend through said traces to said substrate.

45. The system of claim 40, wherein said seats extend through said traces into said substrate.

46. The system of claim 40, wherein said seats partially extend through said traces.

47. The system of claim 40, wherein the system comprises a processor-based computer system.

48. A method for making a carrier for a semiconductor device, said method comprising:

forming a seat with a cut out portion on at least one trace located on a substrate, said seat being sized and configured to receive a conductive connecting structure; and

providing an elastomeric material over said substrate and said trace with a gap at said seat to allow electrical connection of a conductive connecting structure with a semiconductor die.

49. The method of claim 48, further comprising affixing a conductive connecting structure to said cut out portion.

50. The method of claim 49, wherein said affixing comprises affixing a solder ball to said seat.

51. The method of claim 50, further comprising electroplating said seat with one or more metals.

52. The method of claim 51, wherein said electroplating comprises electroplating said seat with nickel and gold.

53. The method of claim 48, further comprising affixing a conductive connecting structure to said semiconductor die.

54. The method of claim 48, wherein said trace is deposited on said substrate.

55. The method of claim 54, wherein said location comprises depositing a plurality of traces.

56. The method of claim 55, wherein said deposition comprises electrolytic deposition.

57. The method of claim 55, wherein said deposition comprises sputter coating.

58. The method of claim 55, wherein said deposition comprises:

laminating a conductive material to said substrate; and

etching said conductive material.

59. The method of claim 48, wherein said forming comprises forming a seat with a cut out portion for each said trace.

60. The method of claim 59, wherein said forming comprises laser drilling.

61. The method of claim 59, wherein said forming comprises mechanical drilling.

62. The method of claim 59, wherein said forming comprises etching.

63. The method of claim 59, wherein said forming comprises mechanical coining.

64. The method of claim 59, wherein said forming comprises laser ablating.

65. A method of making a semiconductor device comprising:

assembling a carrier, said assembling comprising:

forming a seat with a cut out portion on at least one trace located on a substrate, said seat being sized and configured to receive a conductive connecting structure; and

positioning an elastomeric material over said substrate and said trace with a gap at said seat to allow electrical connection of a conductive connecting structure with a semiconductor die; and

electrically connecting said carrier with a semiconductor die.

66. The method of claim 65, further comprising affixing a conductive connecting structure to said cut out portion.

67. The method of claim 66, wherein said affixing comprises affixing a solder ball to said seat.

68. The method of claim 65, further comprising electroplating said seat with one or more metals.

69. The method of claim 68, wherein said electroplating comprises electroplating said seat with nickel and gold.

70. The method of claim 65, wherein said trace is deposited on said substrate.

71. The method of claim 70, wherein said deposition comprises depositing a plurality of traces.

72. The method of claim 71, wherein said deposition comprises electrolytic deposition.

73. The method of claim 71, wherein said deposition comprises sputter coating.

74. The method of claim 71, wherein said deposition comprises:

laminating a conductive material to said substrate; and

etching said conductive material.

75. The method of claim 65, wherein said forming comprises forming a seat with a cut out portion for each said trace.

76. The method of claim 65, wherein said forming comprises laser drilling.

77. The method of claim 65, wherein said forming comprises mechanical drilling.

78. The method of claim 65, wherein said forming comprises etching.

79. The method of claim 65, wherein said forming comprises mechanical coining.

80. The method of claim 65, wherein said forming comprises laser ablating.